Electromagnetic (EM) Crosstalk: Challenges and Trends

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Abstract— With the advent of advanced technologies and System on-Chip (SoC) architectures, ignoring electromagnetic crosstalk is highly risky resulting in significant delays in reaching the market on time as well significant cost over runs. This short article provides a quick definition of electromagnetic crosstalk, in the context of modern SoC designs, and the technology and architectural trends that are fueling its emergence.

Electromagnetic (EM) Crosstalk is an unwanted interference caused by the electric and magnetic fields of one or more signals (aggressors) affecting another signal (victim). This phenomenon is also referred to in the literature as coupling or noise. Crosstalk occurs via two mechanisms: Capacitive crosstalk caused by the electrical field, and inductive crosstalk caused by the magnetic field.

To help understand the complexities of EM crosstalk analysis, let us contrast that problem with that of analyzing capacitive coupling in digital designs using noise analysis tools. Capacitive coupling is stronger at close proximity and fades out at longer distances, so these tools can and do safely ignore coupling between signal lines that are not physically close to each other. In addition, these tools completely ignore inductive magnetic coupling.

The problem of analyzing EM crosstalk is more challenging. First of all the symptoms of the problem do not neatly package themselves into one metric like timing failure – it often manifests as a degradation in some key performance criterion that varies from design to design. Identifying the issue as being crosstalk related is the first challenge. To make matters more complex, EM Crosstalk usually involves unwanted coupling between digital and sensitive analog/RF blocks with either one being the potential aggressor or victim. By its very definition EM crosstalk needs to be identified, debugged and resolved differently in different designs. The existence of this problem is well established and the solution so far has been tricks in architecture in higher layers of hardware or software to prevent modes of operation that trigger the problem. However, this is becoming financially and in some cases, technically untenable as the designs have grown in complexity and speed.

A major complexity associated with EM crosstalk is the staggeringly complex scope of physical structures that need to be handled in order to create a complete EM model of the signal nets of interest. E.g. surrounding nets, plus all the surrounding structures that can contribute to crosstalk including power and ground routing layers, bulk silicon substrate, package layers, bond/bump pads with their routing layers, seal rings, metal fill, de-coupling caps, etc. Note that most of these structures have complex physical layouts and they need to be properly meshed to extract resistance, capacitance, inductance, coupling capacitance, and mutual inductance.

A second complexity factor can be illustrated by considering the following question: Given a potential victim signal, can we analyze EM crosstalk by limiting our focus to a small bounding box in the design? The answer unfortunately is no.

Analyzing the neighborhood of a victim signal works well for electrical capacitive coupling only. However, magnetic field can travel along relatively large loops that are formed by structures outside the immediate neighborhood of a victim signal and can sometimes encircle the whole layout of the chip.

Finally, the output model generated by EM crosstalk tools can be extremely complex because it includes all the nets that contribute to the crosstalk problem plus all the nets and structures that might have an impact on the performance of the circuit. However, the output model must also satisfy the following key criteria to be useful for further processing: (i) easily simulated with a spice-type simulator in a reasonable amount of time, (ii) be suitable for all kinds of non-linear and noise simulations with spice and last but not least, (iii) be easily back-annotated in a rather complex and hierarchical design database that crosses the boundaries of blocks or silicon dies.

What is Fueling the Emerging Need for EM Crosstalk Analysis in SoCs?

The increasing demand for electronic systems with increasing bandwidth and decreasing size puts more high-speed circuitry and high bandwidth channels in ever-closer proximity.

The continuous increase in internal clock frequencies (e.g. 5-10 GHz) and the increase in data rates (e.g. >10Gbps) are fueling the emergence of EM crosstalk issues. Parasitic inductance and inductive coupling that were previously safe to ignore can no longer be ignored. The faster the speed, the louder the crosstalk. It is important to note that a clock signal with fast rise and fall times contains significant harmonic frequency components. So, for example, a clock running at 10GHz has a 5th harmonic frequency component running at 50GHz. Those who target on-chip clock frequencies of 25GHz, will have to think about how to safely model the 3rd harmonic which falls into what microwave design engineers call the “W band”. Therefore, high performance SoC designs start having problems of a “microwave” nature.

System-on-a-chip (SoC) integration places complex high speed digital circuitry, analog and RF blocks very close together. This creates many opportunities for EM crosstalk inside those complex components as well as across various blocks. Note that most EDA tools are geared for a specific design type (digital, analog, RF, etc.) However, as we explained earlier, EM crosstalk is not limited by the boundaries or types of those different design components or the types of analyses that a designer is used to regularly run.

The impact of crosstalk is further exacerbated by the decrease in signal voltage levels driven by lower-power trends in today’s SoC applications.

In addition to the technology trends we discussed, there are many architectural and application-oriented design trends that are contributing to the emergence of EM crosstalk.

Serial buses such as Ethernet, Fiber Channel, and PCI Express capitalize on the robust nature of serial technology, with its interference-canceling differential signaling and jitter-canceling embedded clocking. To achieve their data rates, these buses employ multiple serial lanes that operate in parallel. For example, a 100-Gbps Ethernet employ up to 10 channels at 10 Gbps each or four channels at 25 Gbps. When so many high-speed serial lanes reside in a single system, every lane can be a potential aggressor or a potential victim and this is a true crosstalk nightmare.

There are many other architectural trends that increase the likelihood of EM crosstalk:

- The presence of several high-speed analog blocks such as PLLs and VCOs on the same SoC.
- The presence of multiple high-speed clock networks on the same chip. Not all clocks need to operate at very high frequency, we have seen cases with the victim clock running at 10 GHz and the aggressor was a second clock running at 2GHz.
- RF or high speed analog blocks adjacent to high-speed digital blocks. This situation is very common in most high-performance transceivers. The problem is amplified because they all share ground nets and a common silicon substrate that cannot be tapped to ground as most people still naively think. Silicon substrate remains a key noise-propagation channel between blocks.
- The insertion of seal rings and scribe lines by foundries.
- Low power designs with very small signal-to-noise margins.
- The presence of sensitive control/reset signals that can be erroneously set by glitches caused by crosstalk.
- The use of integrated fan-out wafer-level packaging techniques add another dimension of complexity to the crosstalk problem by bringing multiple dies very close together increasing the likelihood of EM crosstalk.

In conclusion, with the advent of advanced technologies and System on-Chip (SoC) architectures, ignoring electromagnetic crosstalk is highly risky resulting in significant delays in reaching the market on time as well significant cost over runs