Crosstalk Analysis At 7nm

Faster speed and smaller features are increasing the noise volume.

The increasing demand for electronic systems with increasing bandwidth and decreasing size puts more high-speed circuitry and high bandwidth channels in ever-closer proximity.

The continuous increase in internal clock frequencies (e.g. 5 - 10 GHz) and the increase in data rates (e.g. >10Gbps) are fueling the emergence of electromagnetic (EM) crosstalk issues. Parasitic inductance and inductive coupling that were previously safe to ignore can no longer be ignored. The faster the speed, the louder the crosstalk.

It is important to note that a clock signal with fast rise and fall times contains significant harmonic frequency components. So a clock running at 10GHz, for example, has a fifth harmonic frequency component running at 50GHz. Those who target on-chip clock frequencies of 25GHz will have to think about how to safely model the third harmonic, which falls into what microwave design engineers call the "W band." Therefore, high-performance SoC designs start having problems of a "microwave" nature.

System-on-a-chip (SoC) integration places complex high speed digital circuitry, analog and RF blocks very close together. This creates many opportunities for EM crosstalk inside those complex components, as well as across various blocks. Note that most EDA tools are geared for a specific design type, such as digital, analog and RF. But EM crosstalk is not limited by the boundaries or types of those different design components or the types of analyses that a designer is used to regularly run.

The impact of crosstalk is further exacerbated by the decrease in signal voltage levels driven by lower-power trends in today's SoC applications.

In addition to the technology trends we discussed, there are many architectural and application-oriented design trends that are contributing to the emergence of EM crosstalk.

Serial buses such as Ethernet, Fibre Channel, and PCI Express capitalize on the robust nature of serial technology, with its interference-canceling differential signaling and jitter-canceling embedded clocking. To achieve their data rates, these buses employ multiple serial lanes that operate in parallel. For example, a 100-Gbps Ethernet employ up to 10 channels at 10 Gbps each or four channels at 25 Gbps. When so many high-speed serial lanes reside in a single system, every lane can be a potential aggressor or a potential victim and this is a true crosstalk nightmare.

There are many other architectural trends that increase the likelihood of EM crosstalk:

- The presence of several high-speed analog blocks such as PLLs and VCOs on the same SoC.
- The presence of multiple high-speed clock networks on the same chip. Not all clocks need to operate at very high frequency, we have seen cases with the victim clock running at 10 GHz and the aggressor was a second clock running at 2GHz.

- RF or high-speed analog blocks adjacent to high-speed digital blocks. This situation is very common in most high-performance transceivers. The problem is amplified because they all share ground nets and a common silicon substrate that cannot be tapped to ground as most people still naively think. A silicon substrate remains a key noise-propagation channel between blocks.
- The insertion of seal rings and scribe lines by foundries.
- Low power designs with very small signal-to-noise margins.
- The presence of sensitive control/reset signals that can be erroneously set by glitches caused by crosstalk.
- The use of integrated fan-out wafer-level packaging techniques add another dimension of complexity to the crosstalk problem by bringing multiple dies very close together increasing the likelihood of EM crosstalk.
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In conclusion, with the advent of advanced technologies and System on-Chip (SoC) architectures, ignoring electromagnetic crosstalk is highly risky resulting in significant delays in reaching the market on time as well significant cost overruns.