Challenges and Trends in SOC Electromagnetic (EM) Crosstalk

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Abstract—Electromagnetic Crosstalk analysis is emerging as a fundamental necessity as a component of electronic system development. With the advent of advanced technologies and System on-Chip (SoC) architectures, ignoring electromagnetic crosstalk is highly risky resulting in significant delays in reaching the market on time as well significant cost over runs. This paper provides an overview of the state of the practice in electromagnetic crosstalk in the context of modern SoC designs, current industrial trends, and key adoption challenges.

Index Terms—Electromagnetic (EM) Crosstalk, EM Jitter, EM coupling, EM analysis and signoff, post silicon debug, 3D extraction, EM solvers, and EM crosstalk EDA tools.

1. Introduction

Electromagnetic (EM) Crosstalk is an unwanted interference caused by the electric and magnetic fields of one or more signals (aggressors) affecting another signal (victim). This phenomenon is also referred to in the literature as coupling or noise. Crosstalk occurs via two mechanisms: Capacitive crosstalk caused by the electrical field, and inductive crosstalk caused by the magnetic field.

To help understand the complexities of EM crosstalk analysis, let us contrast that problem with that of analyzing capacitive coupling in digital designs using noise analysis tools such as Prime-Time-SI. Table 1 illustrates the differences between capacitive coupling analysis tools used for timing and noise analysis and full EM Crosstalk analysis for performance optimization in mixed-signal and high-speed SOC designs. We should emphasize here that we are not advocating the superiority of one class of tools over the other. Each class has its own application domain and in their respective roles, they are very useful.

Table 1: Comparing Capacitive Coupling Tools to EM Crosstalk Tools

Comparison Criteria	Capacitive coupling tools	EM crosstalk Analysis
Primary Application	Timing and Noise Analysis	EM Crosstalk Analysis
Scope	Digital blocks	SoC Designs with analog, mixed-signal, RF and Digital blocks
Extraction required	R and C for active signal nets plus coupling capacitance between the signal nets. Inductance extraction is not required.	RLCK for all relevant structures in the design including signal nets, power and ground nets, substrate, package layers, passive metal structures, etc.
Required Accuracy Level	Medium accuracy sufficient (e.g., pattern matching)	High accuracy required (e.g. 2.5D or 3D field solver)
Proximity Rule Applies	Yes	No
Type of simulation	Timing simulation	Spice simulation

Noise analysis tools such as Prime-Time-SI focus on the adverse impact on the design performance (e.g., timing) due to unwanted coupling between signal lines via parasitic capacitance in digital designs. Capacitive coupling between the aggressor and the victim is stronger at close proximity and fades out at longer distances, so these tools can and do safely ignore coupling between signal lines that are not physically close to each other. In

addition, these tools completely ignore inductive magnetic coupling.

The problem of analyzing EM crosstalk is more challenging. First of all the symptoms of the problem do not neatly package themselves into one metric like timing failure – it often manifests as a degradation in some key performance criterion that varies from design to design. Identifying the issue as being crosstalk related is the first challenge. To make matters more complex, EM Crosstalk usually involves unwanted coupling between digital and sensitive analog/RF blocks with either one being the potential aggressor or victim. By its very definition EM crosstalk needs to be identified, debugged and resolved differently in different designs. The existence of this problem is well established and the solution so far has been tricks in architecture in higher layers of hardware or software to prevent modes of operation that trigger the problem. However, this is becoming financially and in some cases, technically untenable as the designs have grown in complexity and speed.

Given the narrow/defined scope of the problem that capacitive coupling noise analysis tools are trying to solve, there is no need for such tools to cross design hierarchy boundaries when analyzing capacitive crosstalk. Before running Prime-time SI and similar tools, one needs to extract the resistance and capacitance to ground associated with the signal nets in question, as well as the coupling capacitance between these signals nets. There is no requirement to extract coupling capacitance between the signals nets and other metal structures present in the layout. The level of accuracy required during this extraction step doesn't need to be particularly high to generate reasonable capacitive coupling results, except for very critical applications like memory blocks.

On the other hand, analyzing EM crosstalk is a lot more complex. To illustrate consider the following question: Given a potential victim signal, can we analyze EM crosstalk by limiting our focus to a small bounding box in the design? The answer unfortunately is no. Analyzing the neighborhood of a victim signal works well for electrical capacitive coupling only. However, magnetic field can travel along relatively large loops that are formed by structures outside the immediate neighborhood of a victim signal and can sometimes encircle the whole layout of the chip.

A second major complexity associated with EM crosstalk is the staggeringly complex scope of physical structures that need to be handled in order to create a complete EM model of the signal nets of interest. E.g. surrounding nets, plus all the surrounding structures that can contribute to crosstalk including power and ground routing layers, bulk silicon substrate, package layers, bond/bump pads with their routing layers, seal rings, metal fill, de-coupling caps, etc. Note that most of these structures have complex physical layouts and they need to be properly meshed to extract resistance, capacitance, inductance, coupling capacitance, and mutual inductance.

Finally, the output model generated by EM crosstalk tools can be extremely complex because it includes all the nets that contribute to the crosstalk problem plus all the nets and structures that might have an impact on the performance of the circuit. However, the output model must also satisfy the following key criteria to be useful for further processing: (i) easily simulated with a spice-type simulator in a reasonable amount of time, (ii) be suitable for all kinds of non-linear and noise simulations with spice and last but not least, (iii) be easily back-annotated in a rather complex and hierarchical design database that crosses the boundaries of blocks or silicon dies.

2. The Trends Fueling the Emerging Need for EM Crosstalk Analysis in SoCs.

The increasing demand for electronic systems with increasing bandwidth and decreasing size puts more high-speed circuitry and high bandwidth channels in ever-closer proximity. The continuous increase in internal clock frequencies (e.g. 5-10 GHz) and the increase in data rates (e.g. >10Gbps) are fueling the emergence of EM crosstalk issues. Parasitic inductance and inductive coupling that were previously safe to ignore can no longer be ignored. The faster the speed, the louder the crosstalk. It is important to note that a clock

signal with fast rise and fall times contains significant harmonic frequency components. So, for example, a clock running at 10GHz has a 5th harmonic frequency component running at 50GHz. Those who target on-chip clock frequencies of 25GHz, will have to think about how to safely model the 3rd harmonic which falls into what microwave design engineers call the "W band". Therefore, high performance SoC designs start having problems of a "microwave" nature.

System-on-a-chip (SoC) integration places complex high speed digital circuitry, analog and RF blocks very close together. This creates many opportunities for EM crosstalk inside those complex components as well as across various blocks. Note that most EDA tools are geared for a specific design type (digital, analog, RF, etc.) However, as we explained earlier, EM crosstalk is not limited by the boundaries or types of those different design components or the types of analyses that a designer is used to regularly run.
The impact of crosstalk is further exacerbated by the decrease in signal voltage levels driven by lower-power trends in today's SoC applications.

In addition to the technology trends we discussed, there are many architectural and application-oriented design trends that are contributing to the emergence of EM crosstalk. Serial buses such as Ethernet, Fiber Channel, and PCI Express capitalize on the robust nature of serial technology, with its interference-canceling differential signaling and jitter-canceling embedded clocking. To achieve their data rates, these buses employ multiple serial lanes that operate in parallel. For example, a 100-Gbps Ethernet employ up to 10 channels at 10 Gbps each or four channels at 25 Gbps. When so many high-speed serial lanes reside in a single system, every lane can be a potential aggressor or a potential victim and this is a true crosstalk nightmare.

There are many other architectural trends that increase the likelihood of EM crosstalk:

- The presence of several high-speed analog blocks such as PLLs and VCOs on the same SoC.
- The presence of multiple high-speed clock networks on the same chip. Not all clocks need to operate at very high frequency, we have seen cases with the victim clock running at 10 GHz and the aggressor was a second clock running at 2GHz.
- RF or high speed analog blocks adjacent to high-speed digital blocks. This situation is very common in most high-performance transceivers. The problem is amplified because they all share ground nets and a common silicon substrate that cannot be tapped to ground as most people still naively think. Silicon substrate remains a key noise-propagation channel between blocks.
- The insertion of seal rings and scribe lines by foundries.
- Low power designs with very small signal-to-noise margins.
- The presence of sensitive control/reset signals that can be erroneously set by glitches caused by crosstalk.
- The use of integrated fan-out wafer-level packaging techniques add another dimension of complexity to the crosstalk problem by bringing multiple dies very close together increasing the likelihood of EM crosstalk.

3. A Quick Overview of What is Involved EM Crosstalk Analysis

There are four basic steps involved in doing EM crosstalk analysis as shown in Figure 1:

1. Victim/Aggressor Net Selection:
   In a typical SOC, there are many victim/aggressor pairs that could be analyzed. Analyzing all possibilities may not be feasible due to the resources required. Ideally one should assess the victim/aggressor pairs to identify the ones that most likely exhibit EM crosstalk, so that they can be analyzed first.

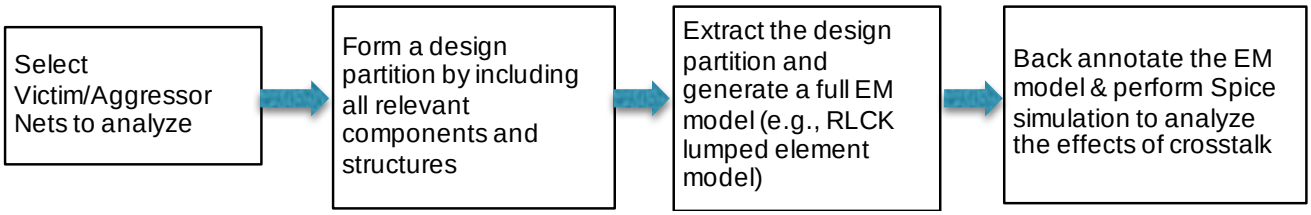

Figure 1: Basic Steps of EM Crosstalk Analysis

2. The Formation of a Design Partition: Given a selected victim and aggressor(s), the next step is to decide what design elements to include in the partition that will be analyzed for EM crosstalk. On one extreme, the entire chip design is too large to analyze in full, but at the same time we must include all design features that may contribute to EM crosstalk. Most EM crosstalk tools available on the market have capacity limitations, and these limitations can result in the exclusion of certain design features that might be crucial to the final result. As we discussed earlier, proximity rules don't apply too well to EM crosstalk analysis as magnetic fields can travel along relatively long loops. Typically, the design partition to be analyzed crosses several design hierarchies, and may include all kinds of structures such as the power and ground nets, package layers, the substrate, coupling caps, fill metal, seal rings, etc.

3. Extraction and Model Generation: In this important step, an accurate extraction is performed on the design partition of step 2 to calculate the resistance, coupling capacitance, inductance, and mutual inductance for all nets, metal structures, etc. The goal is to generate a full and accurate EM model of that design partition. That model can take several forms such as S-parameter model, state-space matrices, rationally fitted model, or a full RLCK model. The latter is preferred to support Spice simulation in the next steps. When extracting a signal net, or a portion of a metal layer, it is usually necessary to break that into multiple segments to be able to accurately extract each of these segments. Calculating the capacitance for example of one of these segments may require very smart meshing to capture curve effects created by the imperfections of advanced technology manufacturing. Hence the extraction engine must be aware of very complex layout effect rules. Without that level of accuracy, the results of crosstalk analysis will not be accurate. Given the size of typical design partitions and all the features that it contains, this places substantial pressure on the extraction engine to handle this capacity, keep the run time reasonable without sacrificing any accuracy. Moreover, the size of the model generated must be compact, otherwise subsequent simulation step becomes impossible. Balancing capacity, speed, accuracy and model-manageability is extremely important to successfully deal with this complex task.

4. Back Annotation and Simulation: In this step the EM RLCK model is back annotated into the design database. Obviously, it is important that the EM tool work seamlessly with other EDA tools used by the SoC design team such as their DRC tool, LVS tool, other extraction tools, etc. Last but not least Spice simulation is performed to observe the impact of crosstalk on the victim signal, or to observe the impact on one of the system performance metrics, such as bit error rate, clock jitter, etc. A key requirement of this step is the availability of a test-bench to drive the simulation.

In many cases, EM Crosstalk analysis is performed post-silicon to diagnose and understand some unexpected silicon measurement. Under these circumstances, the block diagram of Figure 2 illustrates the steps involved.

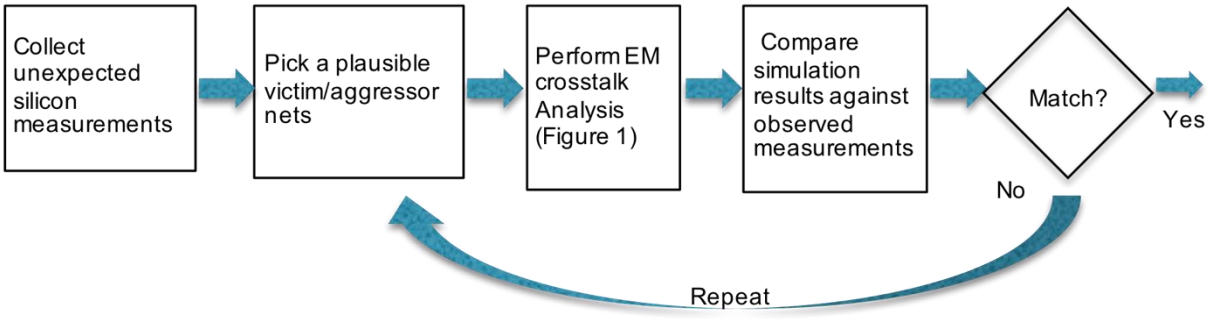

Figure 2: Using EM Crosstalk Analysis to Debug Silicon Issues

Even though there is unexpected observed silicon measurement mismatch, postulating a cause can be very difficult. Determining who is the aggressor or aggressors may not be straightforward. Also, the victim itself may not be obvious because the observed measurement is usually a system performance measurement without a clear indication to what may have caused it. Hence the loop of postulating different causes and analyzing them one by one to get a match between the simulation results and the silicon measurements. Of course there might not be a single cause for the problem which might complicate the debugging process. This flow relies on the expertise of the users and it is iterative in nature. The causes considered are limited by what can be analyzed by the EM Crosstalk analysis tools. Many of the commercially available tools are limited in their ability to extract and model a large design area with all the surrounding layout structures. Not modeling certain structures may lead to erroneous results hiding the real crosstalk effects. There is no guarantee that a "limited and handicapped" iterative process could lead to a real diagnosis of the actual problem. This can obviously lead to delays in getting the product to market and excessive cost over-runs. With time at an extreme premium during these debug situations, the ability of the EM crosstalk tool to handle larger design chunks and to model all the design artifacts can accelerate the identification of the real channels of interference. This can quickly lead to a fix and avoiding costly silicon revs that don't fix the real issue. This is not only valuable, but often it can be described as "priceless and *life-saver!*"

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4. EM Crosstalk Requirements

Table 2 summarizes the essential capabilities that allow designers to tackle EM crosstalk challenges effectively and efficiently.

Table 2: EM Crosstalk Tool Requirements

Ranking Victim/Aggressor net pairs
Large capacity & efficient memory utilization
Ability to do Hybrid Meshing and Modeling
Operates Across Design Hierarchy
Substrate and package layers modeling
Support for Layout-dependent effects (LDE) of advanced technology nodes (10nm, 7nm, etc.)
Generate different output models including physical RLCK Model
Ability to do netlist reduction to reduce the model size without losing accuracy
Ability to back-annotate the extraction model into existing extraction databases created by other tools
Balance capacity, speed and accuracy requirements
Inter-operability with EDA backend tools

It is very important to efficiently model all types of surrounding structures (power/ground nets, substrate, coupling caps, bond pads layers, package layers, seal ring, etc.). Combining high capacity with intelligent handling of all design layout details is crucial to solve EM crosstalk challenges. In advanced technology nodes (16nm and below), it is very important to be able to handle layout-dependent biasing, resistivities and thicknesses. Ignoring these layout-dependent rules can impact the quality of the extraction and can lead to erroneous results.

5. Comparing EM Crosstalk Tools

Most commercial EM solvers are limited by the size of the design that they can handle, or they may take very large amount of time or memory to perform the task. These capacity limitations, memory or runtime constraints often lead to dropping important details about the design and the surrounding environment which in many cases can mask the effects of crosstalk, or can lead to the wrong conclusion. Table 3 compares Helic Exalto tool with Ansys-HFSS tool, considered by many as the reference 3D EM crosstalk tool on the market. As the table clearly demonstrates the Helic tool is more capable of handling SOC EM crosstalk complexity challenges.

Maintaining accuracy is vital when performing EM crosstalk analysis, however, extreme levels of detail may only be needed in critical parts of the layout and not everywhere. Hence, it is often necessary to automatically operate in a hybrid extraction mode to achieve high-accuracy while maintaining reasonable modeling/extraction speed.

Table 3: Helic-Exalto vs Ansys HFSS

	Helic	HFSS
Ranking Victim/Aggressor	Yes	No
Capacity & efficient Memory usage	Very High	Low
Hybrid Modeling	Yes	Limited
Operates Across Design Hierarchy	Yes	No
Substrate modeling	Yes	Limited
Support for Layout-dependent effects (LDE) – resistivities and layer thicknesses	Yes	No
Generate physical RLCK Model	Yes	No
Speed rank	100X faster	1
Accuracy	High	High
Back annotation	Yes	No
Inter-operability with all major EDA tools	Yes	Limited
Market Focus	Analog/ RF Block, multi-blocks, SOC	Analog/RF block, package, PCB

Table 4 finally Compares Helic Exalto extraction engine with the general purpose extraction engines offered by the top 3 EDA vendors. Each of these engines has an add-on option to extract inductance. However, to be fair, we should emphasize that EM crosstalk has not been a targeted application area for these general purpose extraction engines as the table below indicates.

Table 4: Helic Extraction Engine vs the top 3 EDA extraction engines

	Helic	Cadence	Mentor Graphics	Synopsys
	Exalto	Quantus (HF Option)	Calibre PEX (XL Option)	Star-RC (L Option)
True Electromagnetic field solver				
Silicon substrate model				
Capacity & Speed				
Model format	RLCk, RFM, RLCG S-parameters	RLCk	RLC	RLC
Model netlist size				
Compatibility with 3rd party RC extractor	Quantus, Calibre PEX, Star-RC	Only QRC	Only Calibre PEX	Only Star-RC
Application	RF passives, signal and power lines combined	Only signal lines	Only signal lines	Only signal lines
High frequency accuracy (>5GHz)	 to mmWave			

6. Concluding Remarks

In the last few years, we have seen increasing demand by leading semiconductor companies for EM crosstalk analysis tools. There are several factors driving this including: technology shrinking, the increase in **Speed** (both data rates and clock frequencies), **Low-Power,** higher levels of **Integration, and advanced packaging**. In this article we reviewed the complex challenges associated with SOC EM crosstalk analysis and signoff. More importantly we outlined the key requirements for a successful SOC EM crosstalk analysis and signoff tool. Finally we provided some comparative analysis of several commercial EDA tools with respect to their abilities to do EM crosstalk analysis and signoff for complex SOC designs.

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