IP Electromagnetic Crosstalk Requires Contextual Signoff

Continuous advancement in technology scaling is enabling the emergence of high performance application markets such as artificial intelligence, autonomous cars and 5G communication. These electronic systems operate at multi-GHz speed, while consuming the lowest amount of power possible leaving very little margin for error. Chips in these systems are highly integrated with multiple noise sensitive analog and RF blocks in close proximity to high speed digital blocks, making them increasingly susceptible to crosstalk failure.

Electromagnetic (EM) crosstalk is an unwanted interference caused by the electrical (capacitive) and magnetic (inductive) fields by one or more signal (aggressors) affecting another signal (victim). Capacitive coupling is stronger at close proximity and fades out at a longer distance. However, magnetic field can travel along relatively large loop formed by structures outside the immediate neighborhood of the victim signal.

Most of the designs today are built on previous generation and utilizes multiple IPs from internal design teams and outside companies. These reused blocks are verified and validated on its own under the conditions they were designed for, as well as within the context of the previous design. However, once any modification is made to the design, it is no longer safe to assume that the previously signed-off blocks and IPs will operate as expected within the new context.

EM crosstalk travels through substrate, power/ground network, bond/bump pads, decaps, and package layers, so any change in the placement or orientation of the aggressor or its surrounding blocks can alter the behavior of aggressor/victim pair. EM crosstalk is not a standalone metric like timing and its failure is dependent on the particular context that it happens to be in and if the context changes, then the behavior and impact will also change.

Previously, IPs and blocks once signed-off, were considered as black boxes and assumed to function as specified in advanced chips and packages. But when IP or block is placed into a larger design, analysis within the new context needs to be performed to make sure that everything is still functional in the new environment. Designers need a way to quickly analyze as much of the context as possible and come up with a metric that gives them enough confidence that the functionality has been preserved.

But with the complexity of today's designs, traditional tools with limited capacity and scope can no longer produce comprehensive enough results in a reasonable amount of time. Addressing the ever growing EM crosstalk challenges require advancements in tools and methodologies.

Existing crosstalk analysis tools are limited by the capacity of analysis engine, forcing designers to do visual inspection based on experience or pick a small subset of potential aggressor /

victim pair for analysis. This limitation can result in the possibility of missing critical EM crosstalk failures.

An advanced tool will need to be able to quickly analyze very large amount of metal and provide feedback on whether identified victim is safe or if there are any known aggressor that is causing issues. Even with the ability to model enormous amounts of metal, it still will not be possible to cover the entire set of aggressor/victim combinations. Therefore, the tool will also need to be able to determine which combination are critical and how many pairs are good enough to mitigate design failure risks.

Design teams will need to adopt a methodology that incorporates EM crosstalk awareness from early design and throughout every stage as design matures to ensure that EM crosstalk are within specification at every phase of the design. This way, any problem that's encountered will be incremental and can be relatively easy to fix. If EM crosstalk is not considered until the end of the design, it will be much more difficult to detect, debug and fix, and possibly result in redesign.

Growing complexity and increasing frequency is creating greater opportunity for EM crosstalk failures. To effectively address this critical challenge, designers need to raise the level of abstraction by looking at the design from multi-block-level and chip-level while maintaining sufficient granularity to capture the problems that is caused by its context.